

*A1 end*

depositing a BARC layer over said hardmask and within said via, wherein said BARC layer is significantly thicker within said via than over said hardmask; forming a trench pattern over said BARC layer; and etching a trench in said intrametal dielectric layer, wherein said etching a trench step further removes at least a portion of said BARC layer within said via.

Please add the following claims:

*Sub 3*

10. A method of fabricating an integrated circuit, comprising the steps of: forming an interlevel dielectric layer over a semiconductor body; forming a shelf layer over said interlevel dielectric layer; forming an intrametal dielectric layer over said shelf layer; forming a hardmask over said intrametal dielectric layer; forming a via pattern over said hardmask; selectively etching a via through said hardmask; extending said via by selectively etching said intrametal dielectric layer and said shelf layer; depositing a BARC layer over said hardmask and within said via after said extending said via step; forming a trench pattern over said BARC layer; and etching a trench in said intrametal dielectric layer, wherein said etching a trench step further removes at least a portion of said BARC layer within said via.

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11. A method of fabricating an integrated circuit, comprising the steps of: forming an interlevel dielectric layer over a semiconductor body; forming an intrametal dielectric layer over said interlevel dielectric layer; forming a hardmask over said intrametal dielectric layer; forming a via pattern over said hardmask; selectively etching a via through said hardmask; extending said via by selectively etching said intrametal dielectric layer and said interlevel dielectric layer;

depositing a BARC layer over said hardmask and within said via, after the extending said via step;

forming a trench pattern over said BARC layer; and

etching a trench in said intrametal dielectric layer, wherein said etching a trench step further removes at least a portion of said BARC layer within said via.

12. The method of claim 11, further comprising the steps of forming a shelf layer between said interlevel dielectric layer and said intrametal dielectric layer; and extending said via by selectively etching through said shelf layer using said via pattern after said etching a via step.

13. The method of claim 11, wherein said depositing a BARC layer step fills said via to a level approximately even with a height of said interlevel dielectric.

14. The method of claim 11, further comprising the step of removing a remaining portion of said BARC layer after said etching a trench step.